

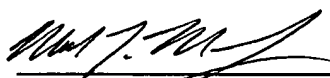


possibly be in existence. Citation of any document herein is not to be construed as an admission that any subject matter disclosed in the document is necessarily within the inventive field of endeavor, that any disclosure is necessarily prior in time to a particular date which may be relevant to the instant patent application, and/or that any disclosure is otherwise necessarily prior art with respect to the instant invention.

Applicant also respectfully reserves the right to later set forth how the instant invention is distinguished over the disclosure of any document or other art, including the disclosure of those documents discussed herein, that may be cited by the Examiner in rejecting a claim in the instant patent application.

As a RCE was filed no fee is believed necessary. If a fee is required, please charge Deposit Account No. 50/1039.

Respectfully submitted,



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LIST OF PUBLICATIONS  
CITED BY APPLICANT

Atty Docket No.  
SEL 239

Serial No.  
09/782,239

Applicant  
Toshimitsu KONUMA  
et al

Filing Date  
February 13, 2001

Group  
2814

**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
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**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NUMBER	DATE	APPLICANT	English Abstract	English Trans.	FILING DATE
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	EP 0 768 352	04/16/97	Hitachi Chem Co.			06/30/95
	EP 0 881 668	12/02/98	Dow Corning Toray			05/27/98
	A2		Silicone Co. Ltd.			
	EP 0 893 485	01/27/99	Sumitomo Chem Co.			07/22/98
	EP 0 899 987	03/03/99	TDK Corp.			08/28/98

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

(Include name of author (in CAPITAL LETTERS), title of article or item (book, magazine, journal, serial, symposium, catalog, etc.) date, pages(s), volume-issue number(s), publisher, city and/or country where published).

- 1) European Search Report re application no. EP 03 02 0964, mailed December 3, 2003.
- 2) FRITSCH, U. et al, "A Submicron CMOS Two Level Metal Process with Planarization Techniques," V-MIC Conf., June 13-14, 1988 IEEE, pp. 69-75 (1988).
- 3) IBARAKI, N. et al, "A New a-Si TFT with SiO<sub>2</sub>/SiN<sub>x</sub> Gate Insulator for 10.4 inch LCDs," Proceedings of the International Display Research Conference, IEEE, pp. 97-100, (1991).
- 4) PRAMANIK, D. et al, "A High Reliability Triple Metal Process for High Performance Application Specific Circuits," VLSI Multilevel Interconnection Conference, June 11-12, 1991, pp. 27-33, (1991).

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